

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/730,896	PAWLOWSKI, J. THOMAS	
Examiner		Art Unit		Page 1 of 1
Paul R. Myers		2112		

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*	B	US-2003/0041223	02-2003	Yeh et al.	711/167
*	C	US-2003/0158981	08-2003	LaBerge, Paul A.	710/100
*	D	US-6,584,526	06-2003	Bogin et al.	710/124
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	A 500-MHz 4-Mb CMOS Pipeline-Burst Cache SRAM with Point-to-Point Noise Reduction Coding I/O
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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